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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/623,234

07/18/2003

Jeffrey S. Kinne

EMC2-144PUS

2729

45456 7590 05/31/2007

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EXAMINER

RABOVIANSKI, ANTON I

ART UNIT

PAPER NUMBER

2188

MAIL DATE

DELIVERY MODE

05/31/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/623,234	<b>Applicant(s)</b> KINNE, JEFFREY S.	
	<b>Examiner</b> Anton Rabovianski	<b>Art Unit</b> 2188	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 December 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some    \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This Office Action is responsive to the Application filed on 07/18/2003.

Claims 1-2 are presented for examination. Claims 1-2 are pending.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaytan et al. (US 5,638,367).

With respect to claim 1, the Gaytan et al. reference teaches a system for storing a block of data, such block of data comprising different packets of data stored in correspondingly different sections of a memory (fig. 1), and for gathering selected portions of the stored packets and then transferring the selected portions of the gathered packets into a transmitted block of data having the selected portions appended contiguously one to the other (col. 1, lines 28-39), such memory storing the packets in word-based locations, the word-based locations having a common word width, W, the stored packets have a variable number of bytes, the bytes of the gathered selected portions of the stored packets being offset from initial byte positions of the stored packets (col. 6, lines 34-67 and col. 9, lines 31-67), the packets having variable offsets (fig. 1, 6a and 7a), such system comprising:

a sampling register (fig. 1, fig. 3 and fig. 6a, i.e. there must be a register between host memory 395 and word packing circuit 600 in fig. 3) having W byte locations for storing W bytes read from a selected one of the word-based locations of the memory, such read bytes being bytes of a currently gathered one of the packets (col. 6, lines 34-44);

a shifter (fig. 6a, el. 610 and 615) for shifting the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently gathered one of the packets and the number of bytes in a prior gathered one of the packets (col. 6, lines 53-65);

an accumulator register (fig. 6b, el. 660) having W byte locations for storing the shifted bytes in response to a clock pulse (col. 9, lines 43-44);

a staging register (fig. 6b, el. 665) having W byte locations, for storing the bytes stored in the accumulator register in response to a subsequent clock pulse (col. 9, lines 44-47); and

a multiplexer (fig. 6b, el. 675) having a W sections, each of the W sections being coupled to a corresponding one of the W byte locations of the accumulator register and a corresponding one of the W byte locations of the staging register, each one of the sections coupling to an output thereof the byte location of the accumulator register or the byte location of the staging register selectively in accordance with the number of bytes in the prior gathered ones of the packets and the number of bytes being gathered from the currently gathered one of the packets (col. 9, lines 31-67 and col. 10, lines 25-30) to provide at an output of the multiplexer bytes to be transmitted as the transmitted

block of data having the selected portions appended contiguously one to the other (fig 1 and fig. 7a-7i).

Regarding claim 2, Gaytan et al. teach a system for distributing different packets of data stored in continuous locations of a memory (fig. 1), such memory storing the packets in word-based locations, the word-based locations having a common word width,  $W$ , the stored packets have a variable number of bytes, the bytes of the distributed packets to be offset from initial byte positions (col. 6, lines 34-67 and col. 9, lines 31-67), the offsets being variable (fig. 1, 6a and 7a), such system comprising:

- a sampling register (fig. 1 and fig. 6a, i.e. there must be a register between host memory 395 and word packing circuit 600 in fig. 3) having  $W$  byte locations for storing  $W$  bytes read from a selected one of the word-based locations of the memory, such read bytes being bytes of a currently distributed one of the packets (col. 6, lines 34-44);

- a shifter (fig. 6a, el. 610 and 615) for shifting the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently distributed one of the packets and the number of bytes in a prior distributed one of the packets (col. 6, lines 53-65);

- an accumulator register (fig. 6b, el. 660) having  $W$  byte locations for storing the shifted bytes in response to a clock pulse (col. 9, lines 43-44);

- a staging register (fig. 6b, el. 665) having  $W$  byte locations, for Storing the bytes stored in the accumulator register in response to a subsequent clock pulse (col. 9, lines 44-47); and

a multiplexer (fig. 6b, el. 675) having a W sections, each of the W sections being coupled to a corresponding one of the W byte locations of the accumulator register and a corresponding one of the W byte locations of the staging register, each one of the sections coupling to an output thereof the byte location of the accumulator register or the byte location of the staging register selectively in accordance with the number of bytes in the prior distributed ones of the packets and the number of bytes being distributed from the currently distributed one of the packets-to provide at an output of the multiplexer (fig. 1; fig. 7a-7i; col. 9, lines 31-67 and col. 10, lines 25-30).

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kaganoi et al. (US 6,026,450) disclose a data transfer control system which uses fields of a table to control the data transfer. Turner et al. (US 6,865,656) disclose a system for efficient transfer of data between custom application specific integrated circuit hardware and an embedded microprocessor. Yee et al. (US 6,466,581) disclose a multistream data packet transfer apparatus that pack data received from different fragments of memory as a single packet for use by a DSP. Padmanabhan et al. (US 6,567,902) disclose a system for packing data into a destination register.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anton Rabovianski whose telephone number is 571-270-1026. The examiner can normally be reached on M-Th 9:00am-7:30pm EST.

Art Unit: 2188

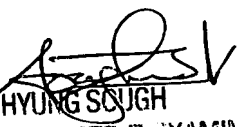
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AR

Anton Rabovianski

May 21, 2007

  
HYUNG SOUGH  
SUPERVISOR/PATENT EXAMINER  
5-29-07